

Fig. 1

Fig. 2

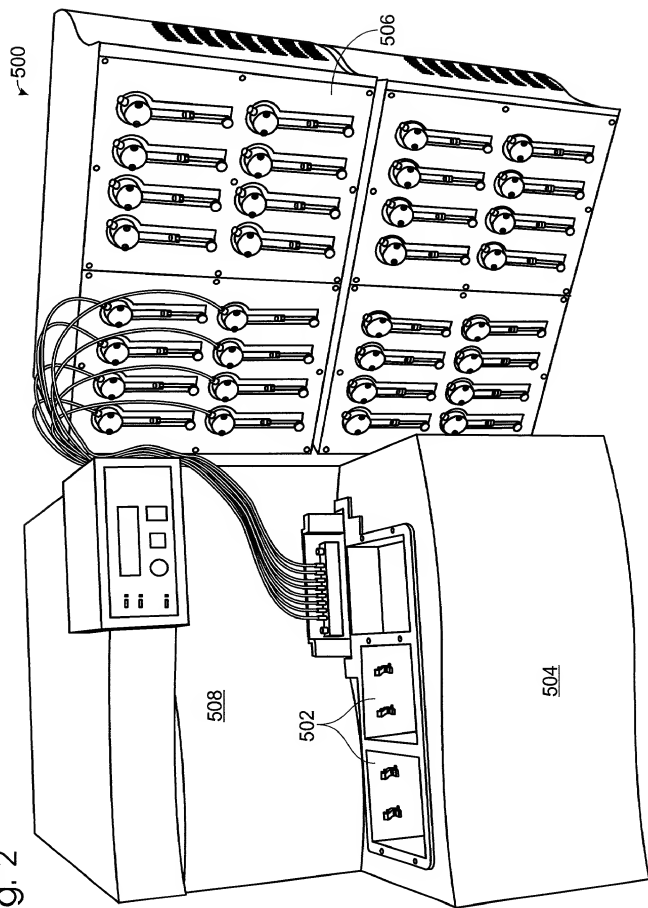


Fig. 3

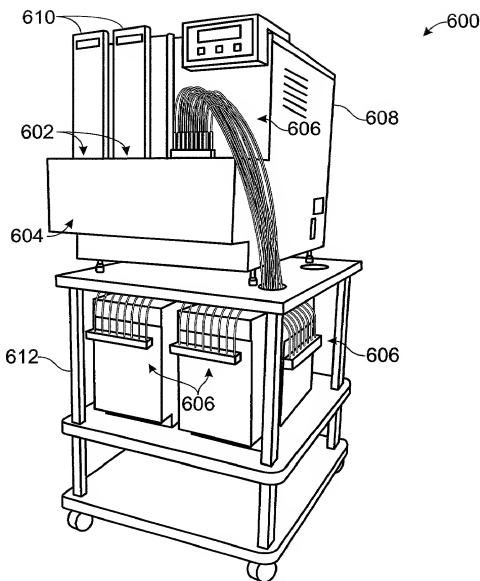
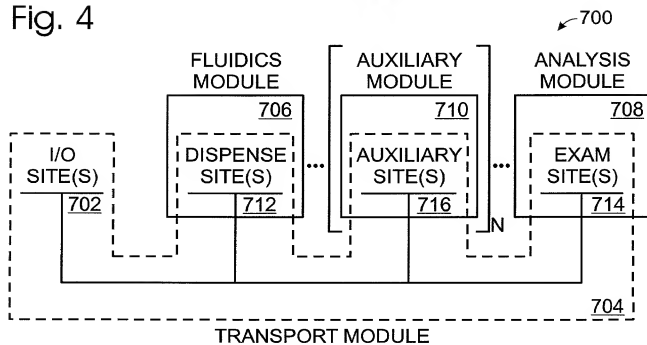
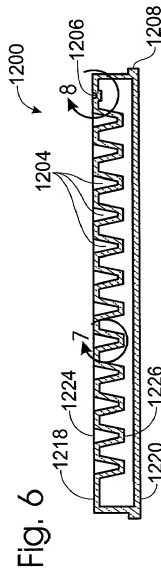
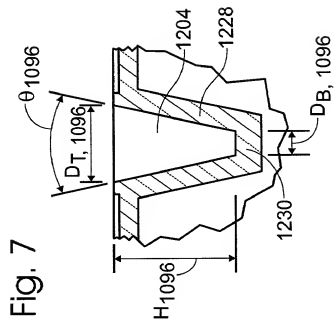
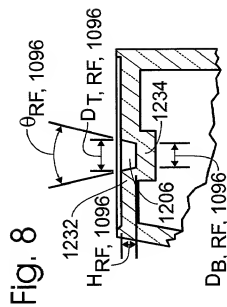
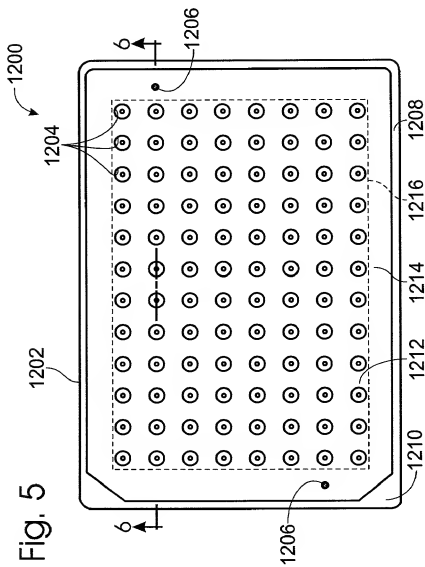


Fig. 4





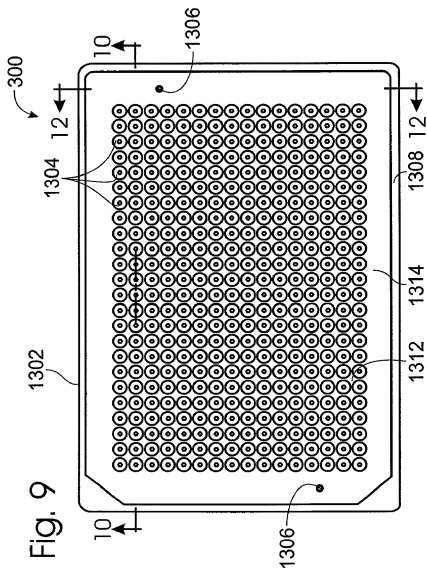


Fig. 12

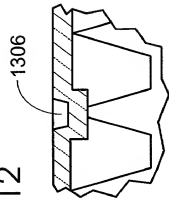


Fig. 11

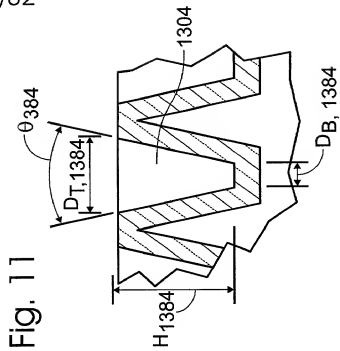


Fig. 10

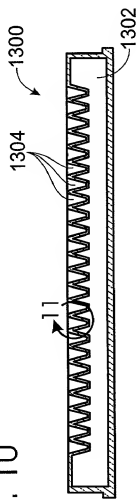


Fig. 13

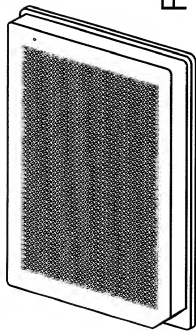


Fig. 15

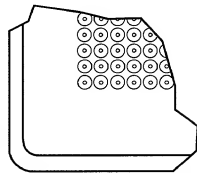


Fig. 17

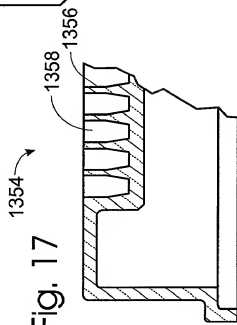


Fig. 14

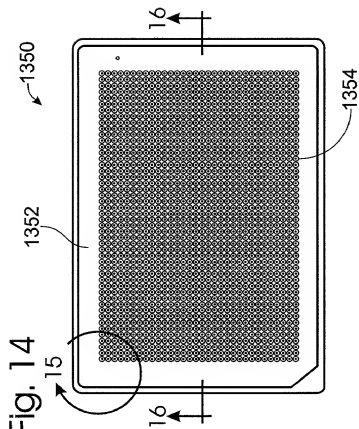
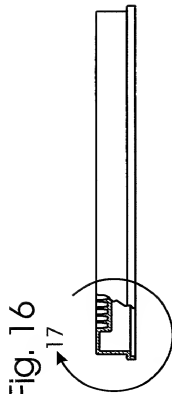


Fig. 16



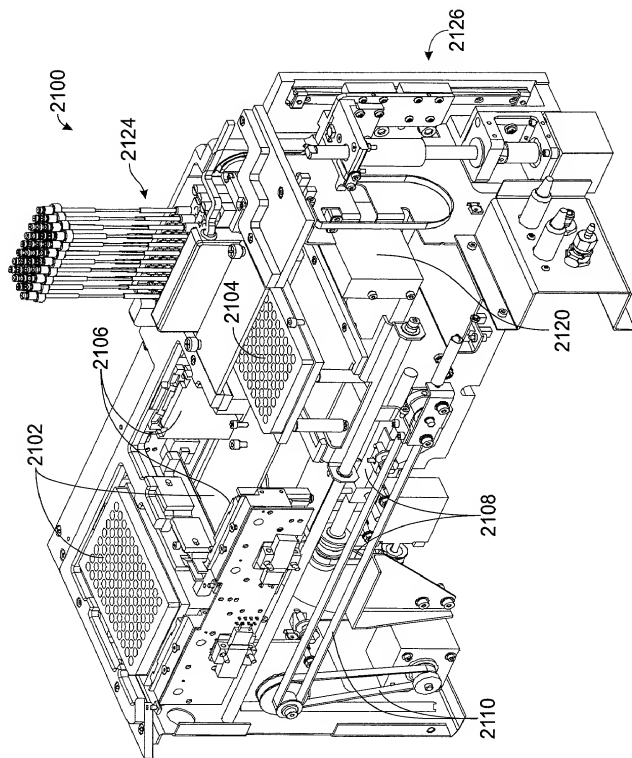


Fig. 18

Fig. 19

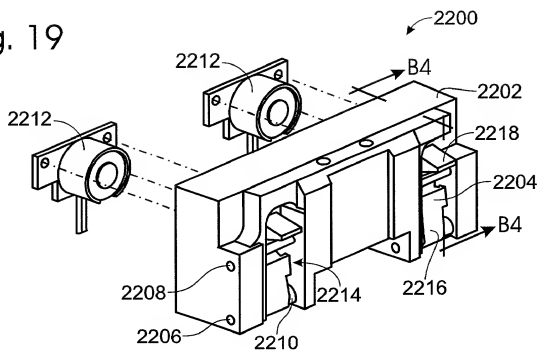


Fig. 20

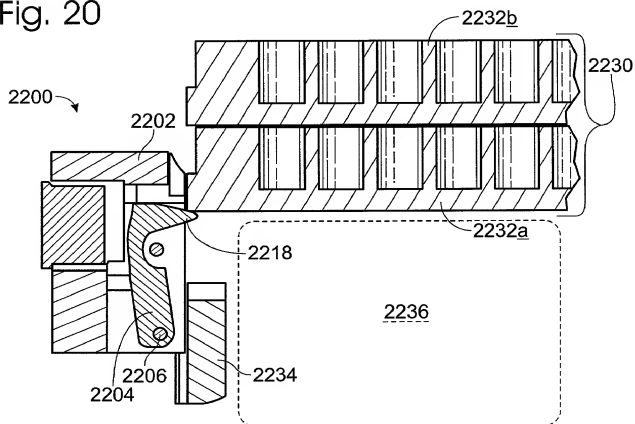




Fig. 21 (INPUT CYCLE)

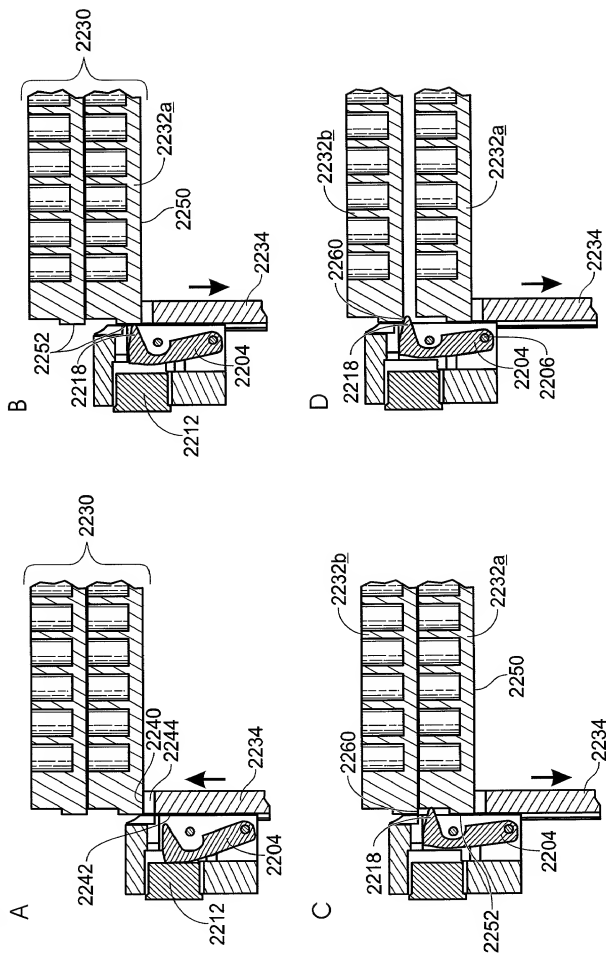


Fig. 22 (OUTPUT CYCLE)

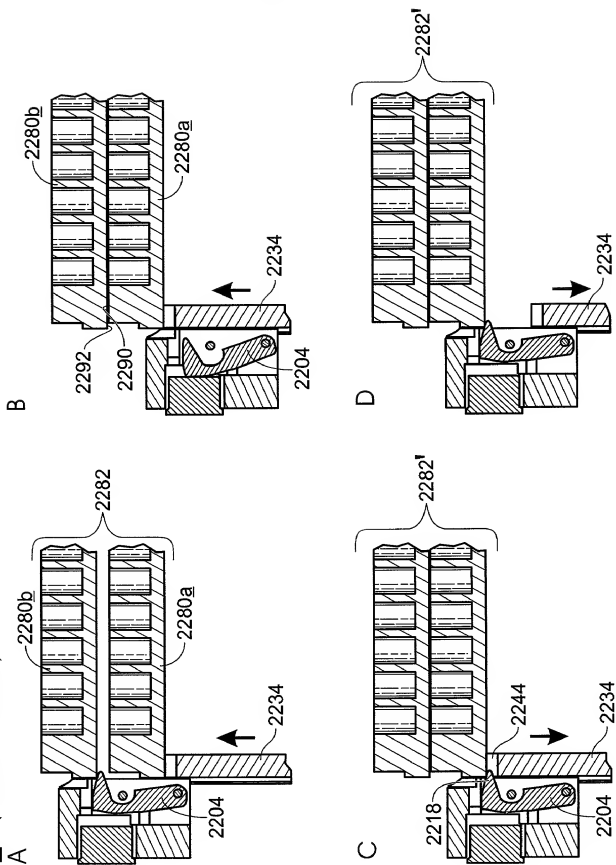
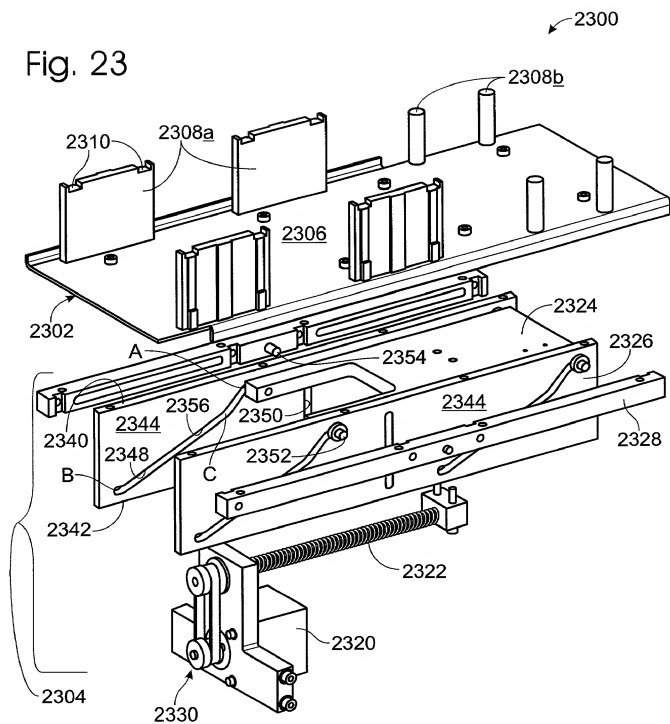


Fig. 23



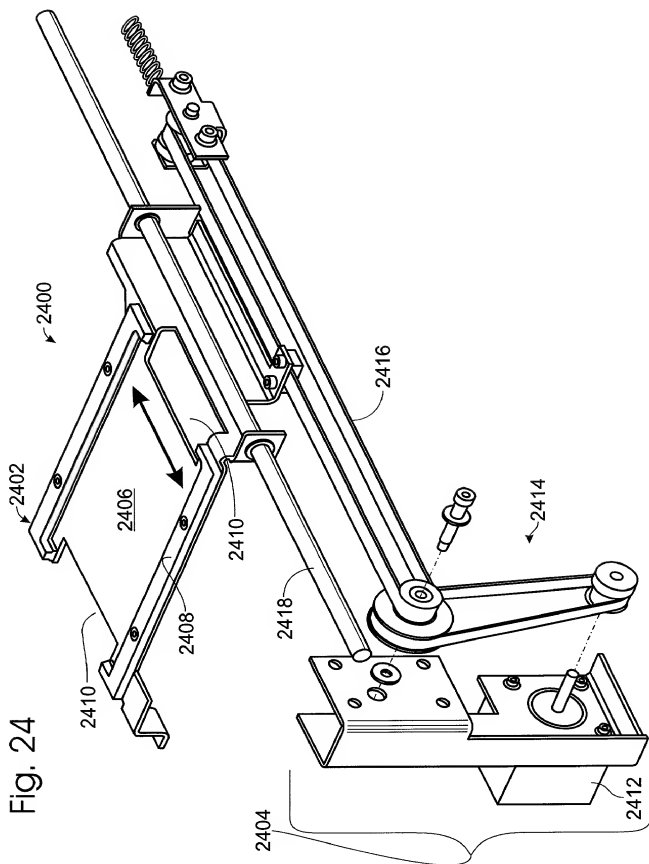


Fig. 25

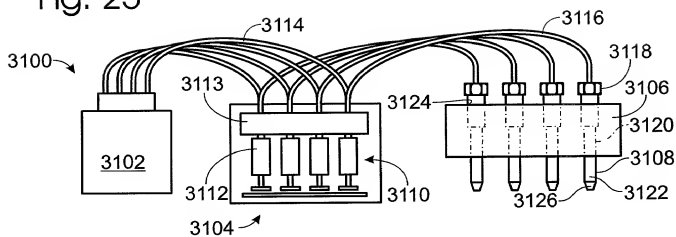


Fig. 26

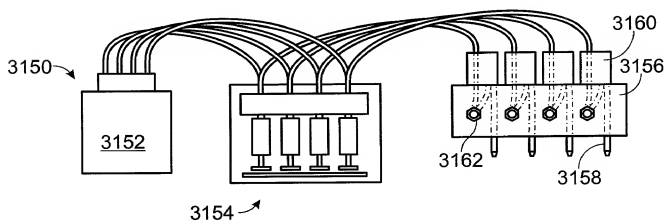


Fig. 27

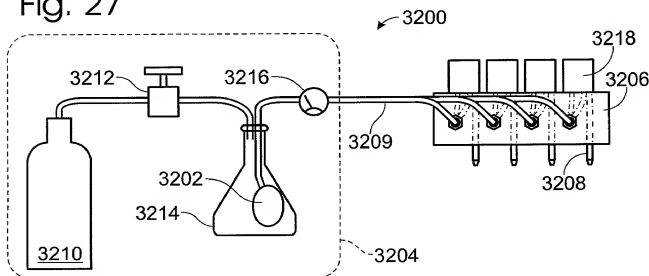


Fig. 28

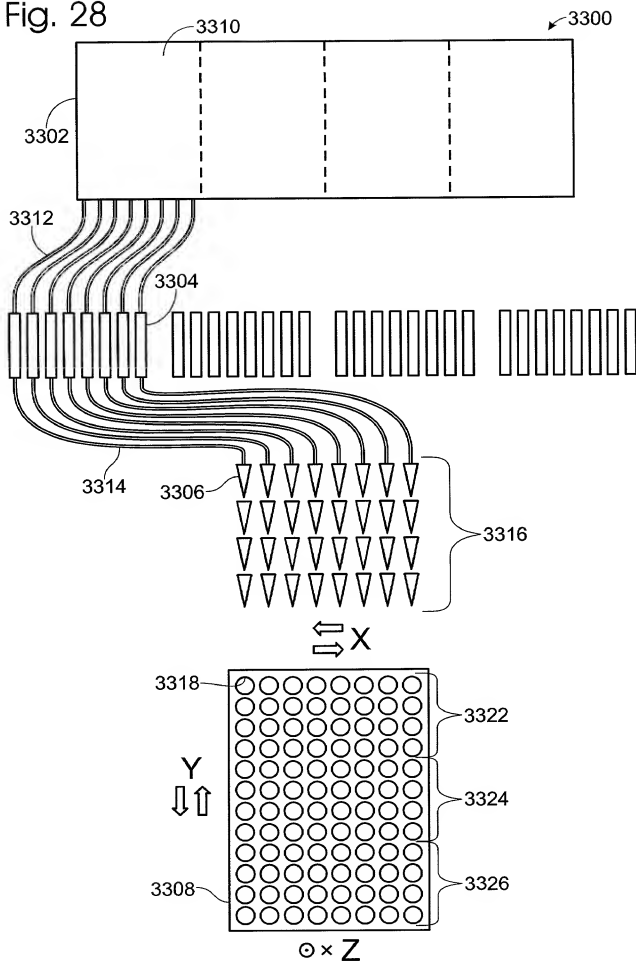


Fig. 29

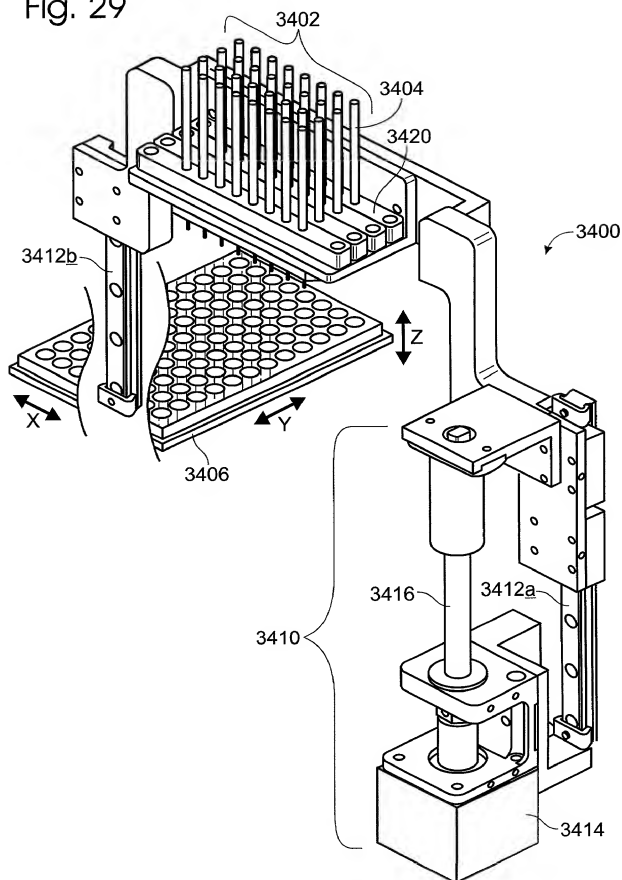


Fig. 30

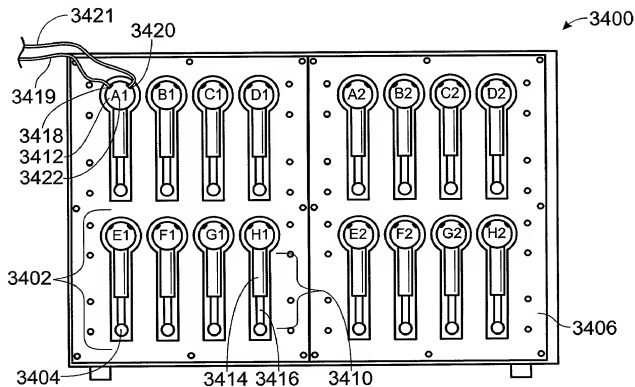


Fig. 31

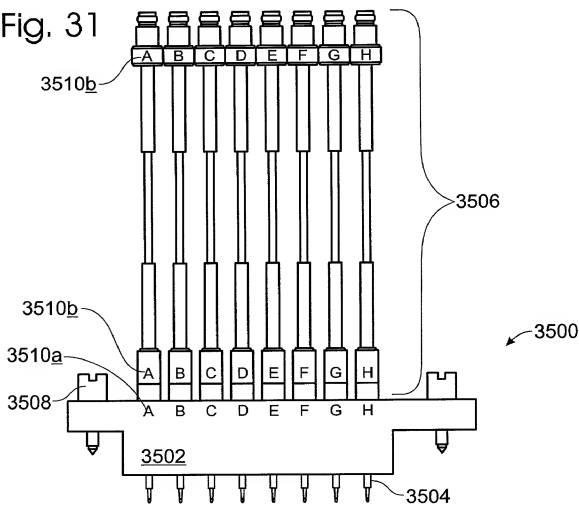




Fig. 32

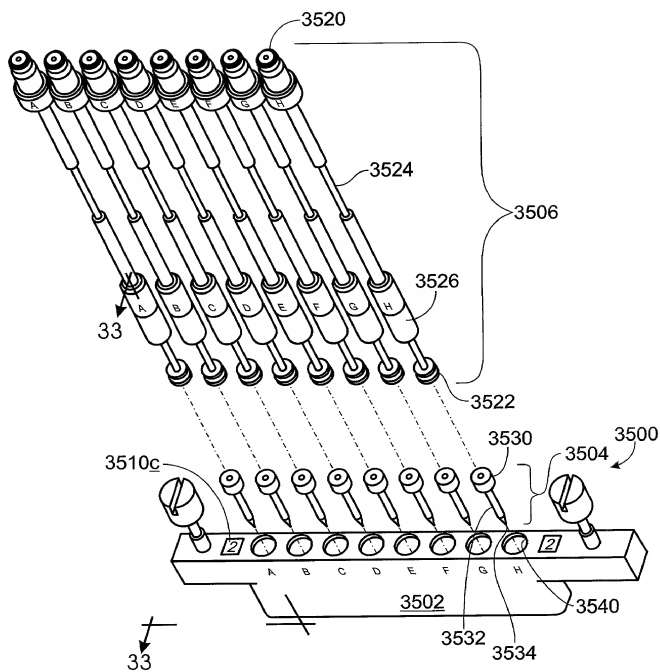


Fig. 33

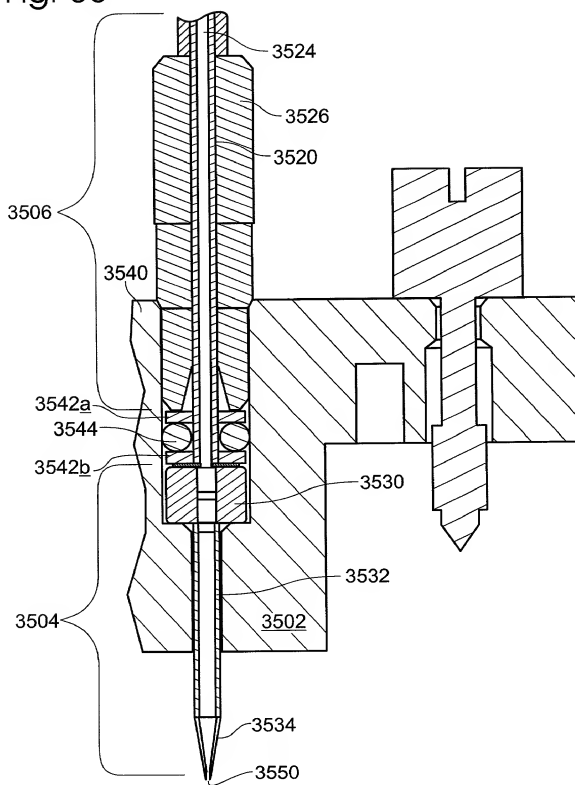


Fig. 34

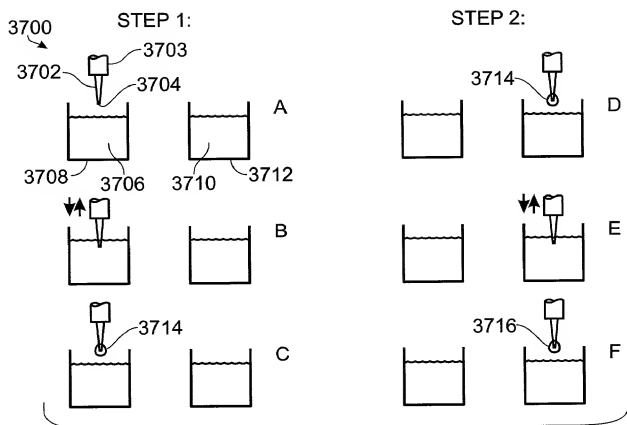


Fig. 35

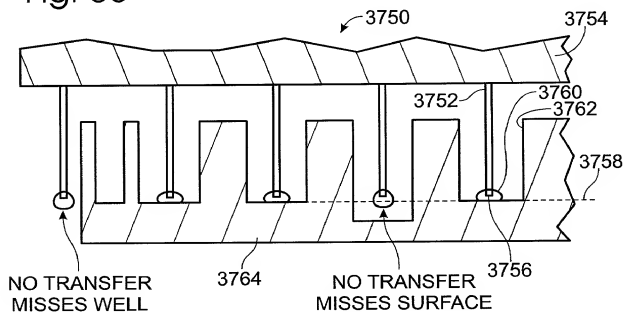


Fig. 36

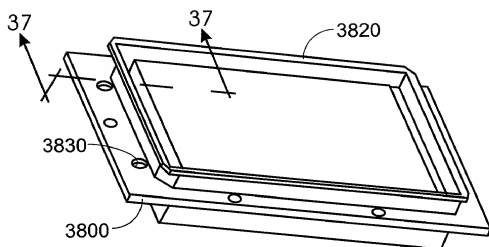


Fig. 37

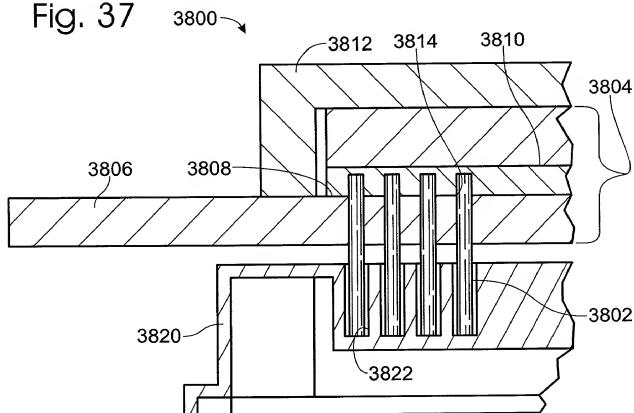


Fig. 38

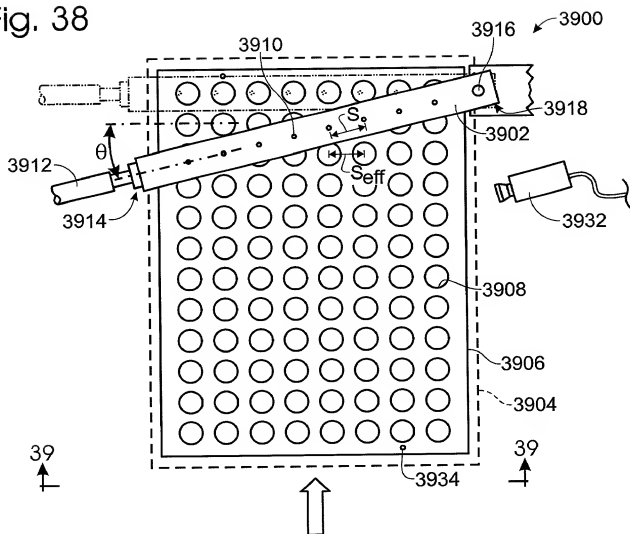


Fig. 39

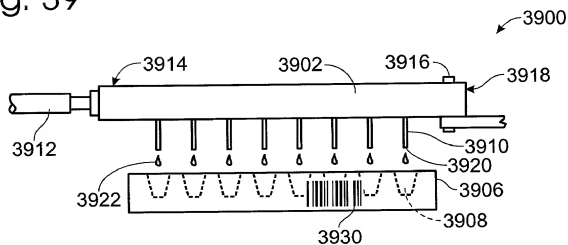


Fig. 40

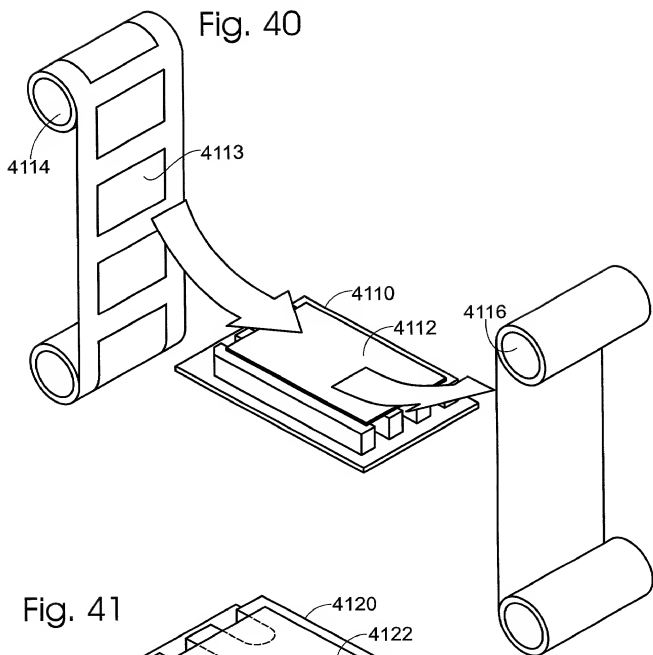


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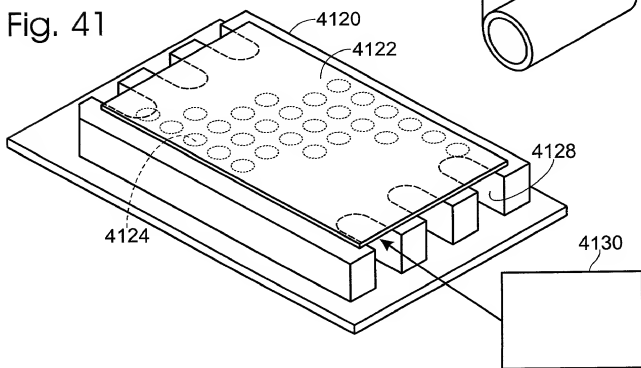


Fig. 42

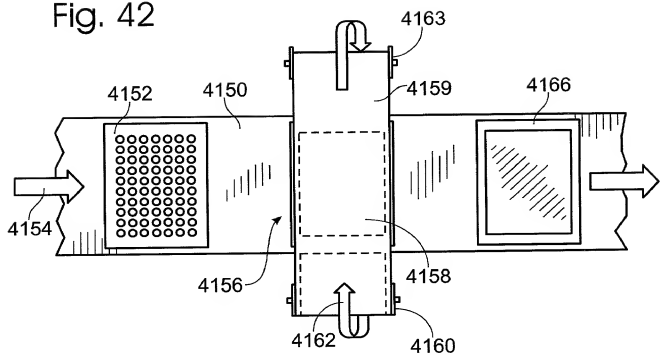


Fig. 43

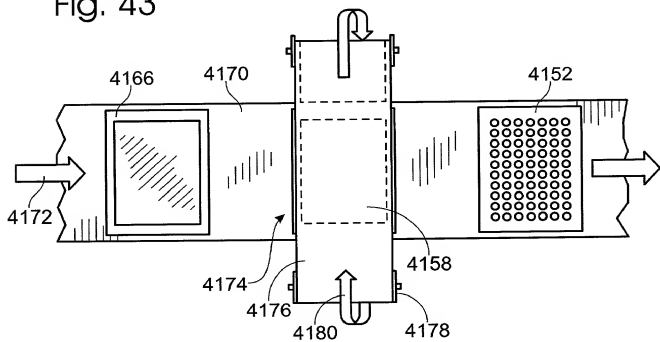


Fig. 44

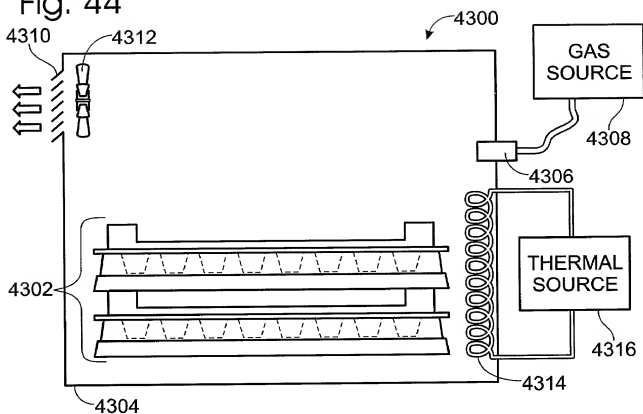


Fig. 45

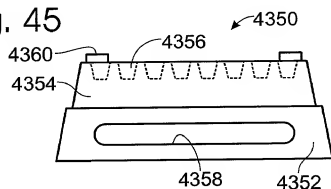


Fig. 46

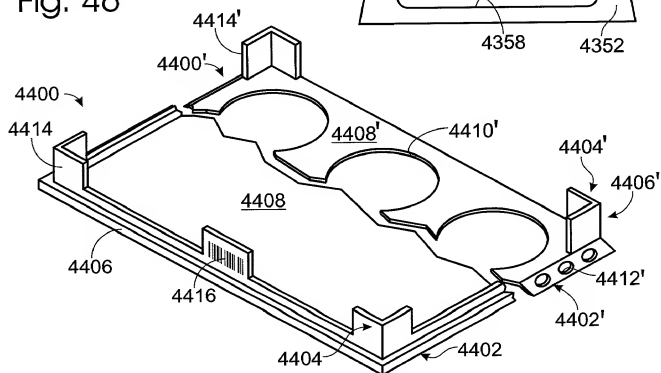




Fig. 47

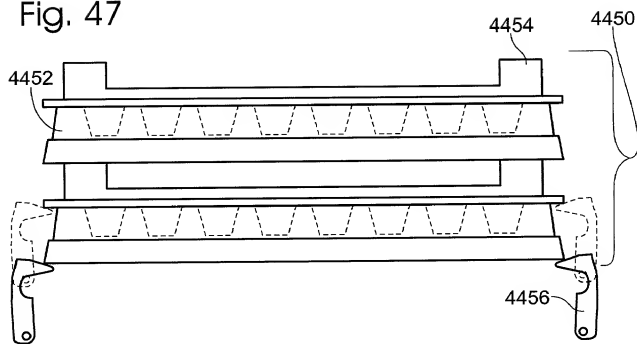
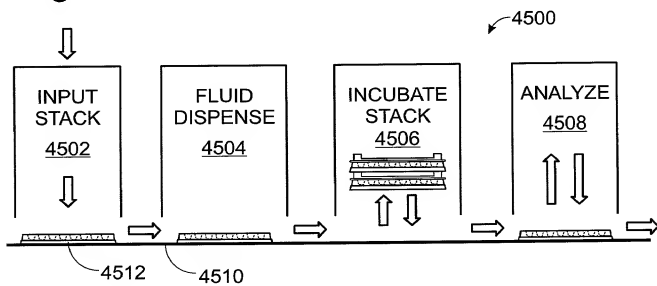


Fig. 48



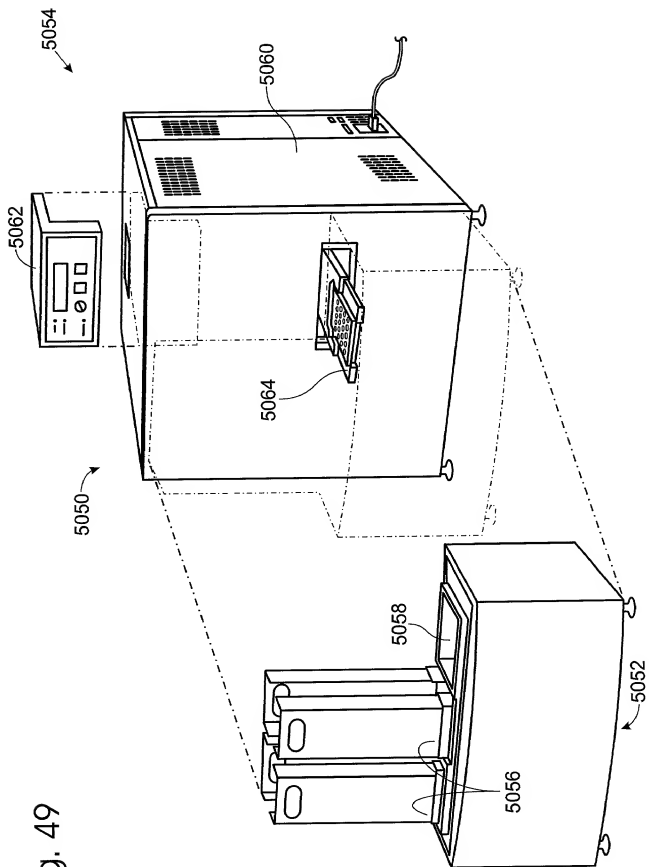


Fig. 49

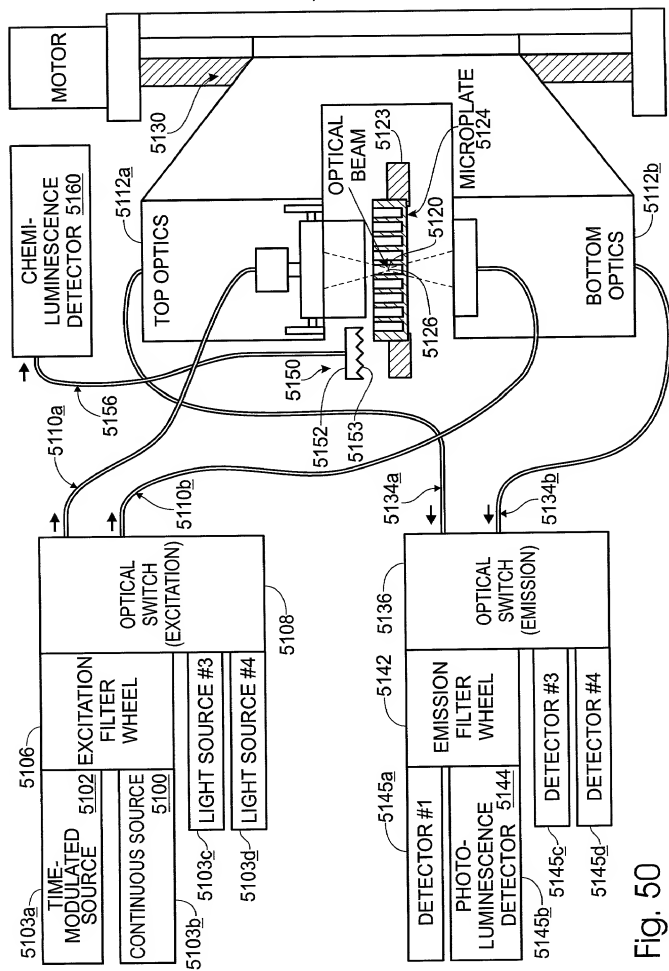


Fig. 50

Fig. 51

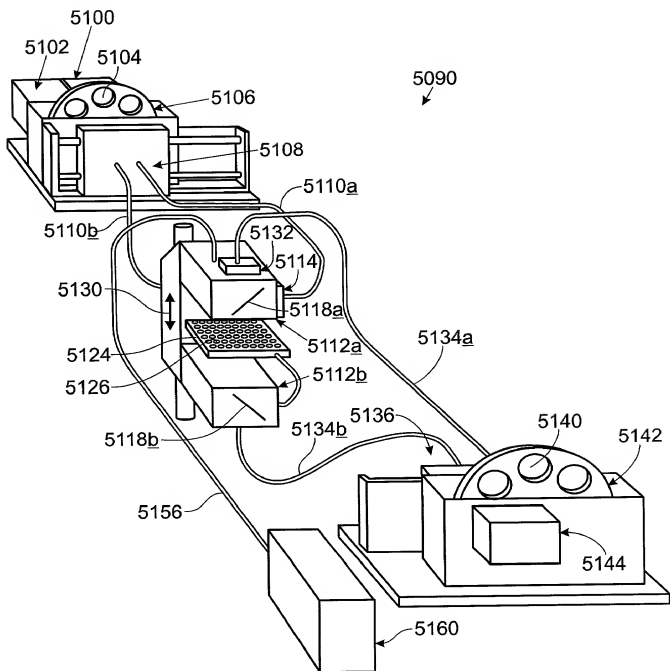


Fig. 52

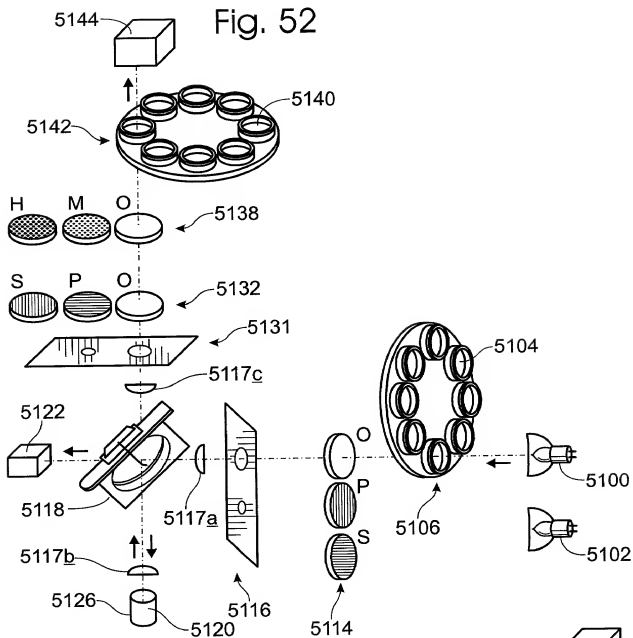


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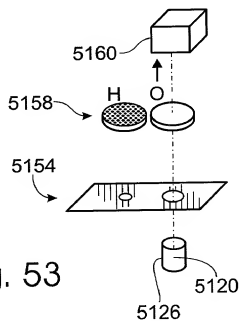


Fig. 54

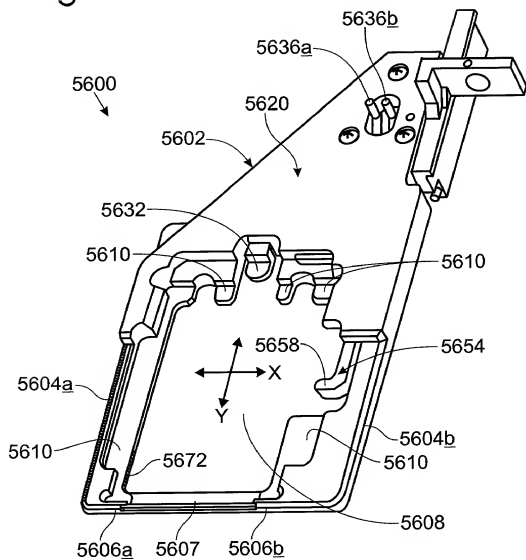


Fig. 55

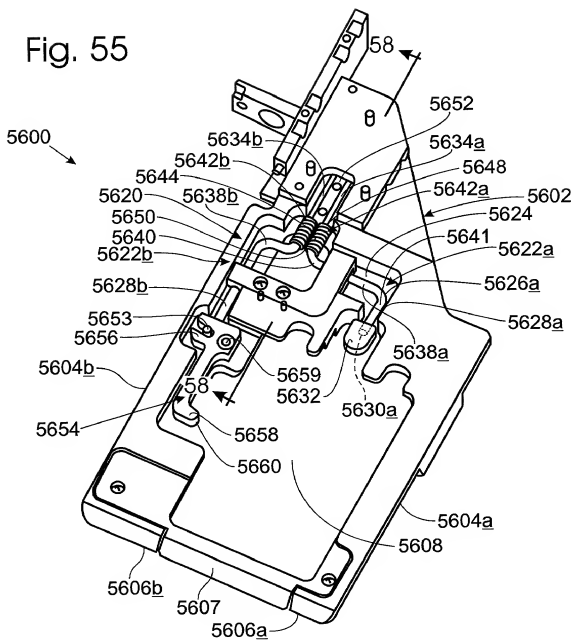


Fig. 56

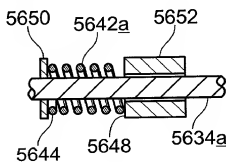


Fig. 57

